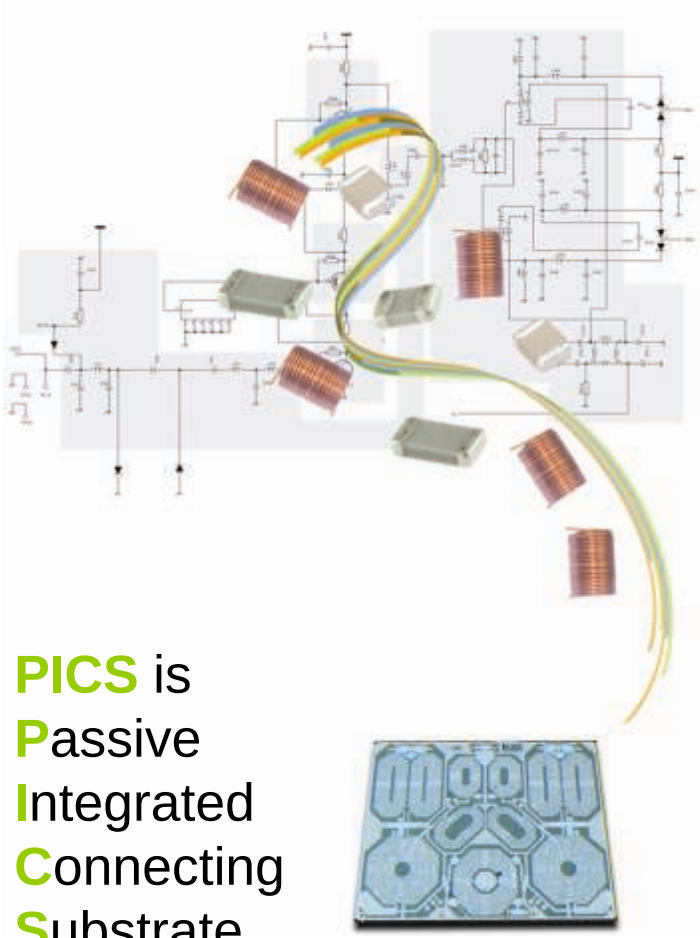
3D Capacitors : manufacturing and applications

Catherine Bunel

R&D Director

ipdia, a new company based on a unique technology



PICS is
Passive
Integrated
Connecting
Substrate

IPDIA's "PICS" passive integration (IPD) technology is a highly efficient way to integrate 10's to 100's of passive components such as Resistors, Capacitors, Inductors and Zener Diodes in a single Silicon die.

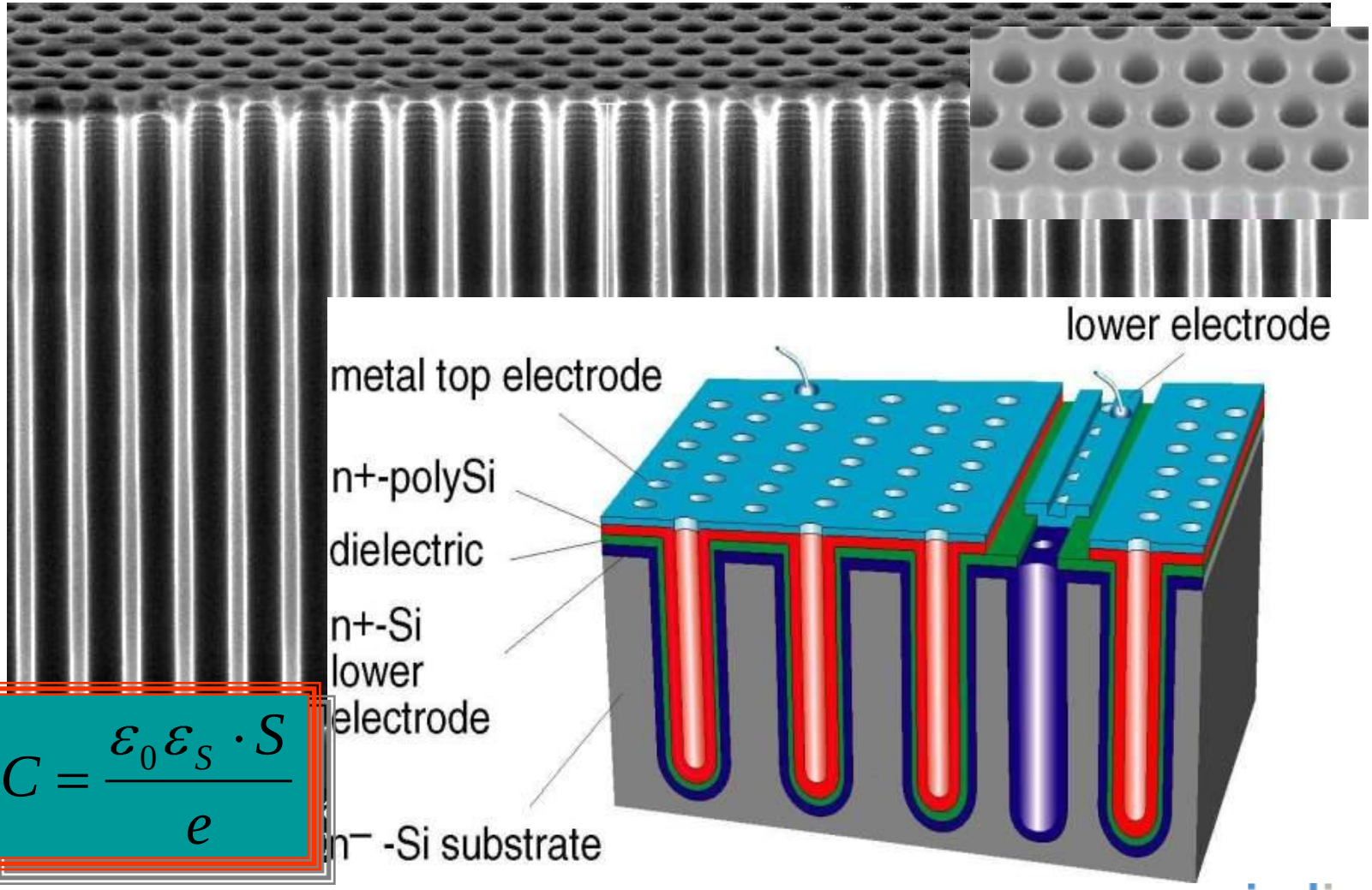
IPDIA's Value proposition is :

Miniaturization

Performances

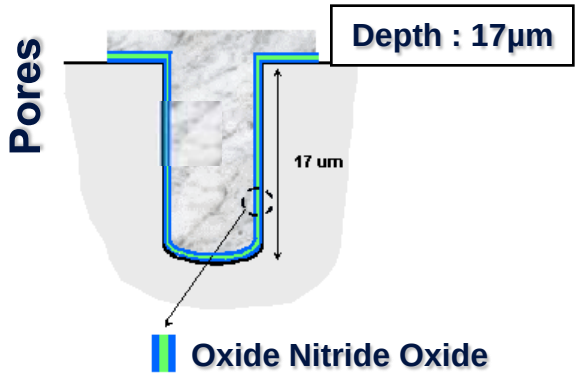
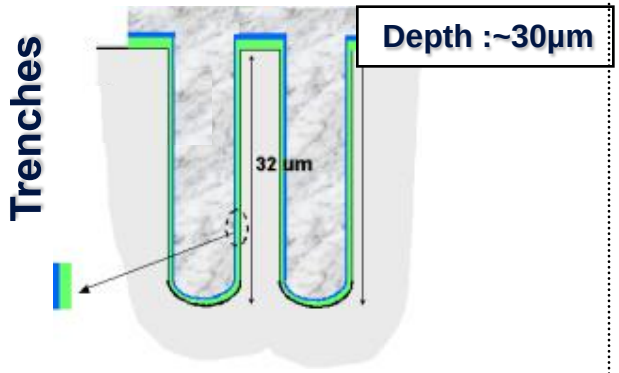
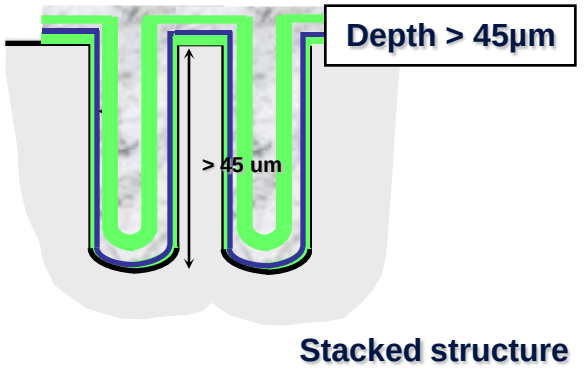
Cost

PICS High Density Trench Capacitor



$$C = \frac{\varepsilon_0 \varepsilon_S \cdot S}{e}$$

Characteristics of the first three generations of PICS

		PICS1	PICS2		PICS3	
Architecture						
Electrical	PICS Cap (nF/mm²)	25	x 3	80	x 3	250
	VBD PICS (V)	30	x 0.5	16	x ~0.8	13

- Increase pore aspect ratio
- Optimize dielectric thickness

- Increase pore aspect ratio
- stacked structure

ipdia

$$C = \frac{\varepsilon_0 \varepsilon_S \cdot S}{e}$$

Capacitor density increase

Increasing εs

High-k materials (ALD, MOCVD, Sol gel)

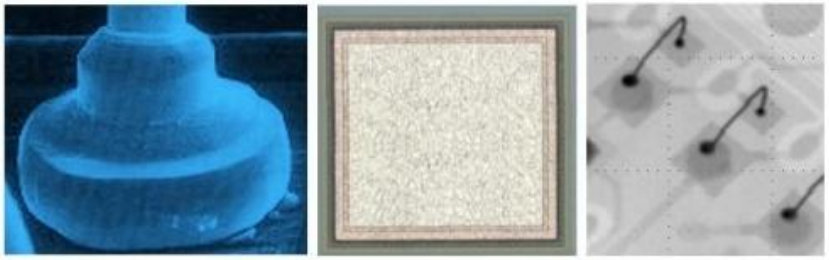
Increasing capacitor surface (S)

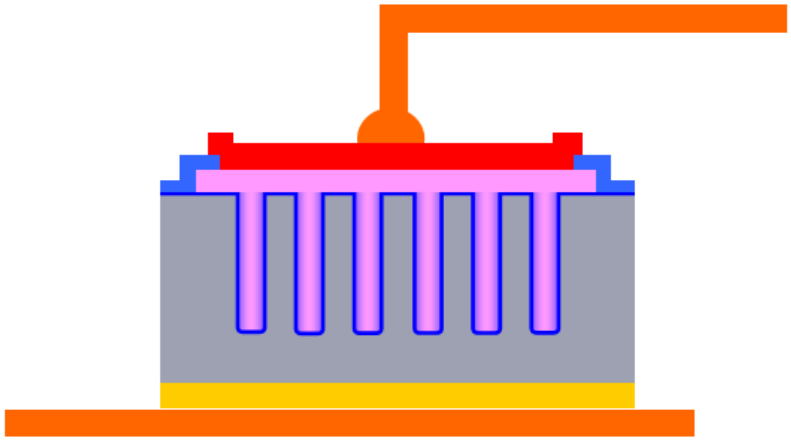
Deeper pores, new pore shapes, more stacks…

Thinning dielectric (e)

Limited to BV & lifetime requirements

The Vertical Cap High Voltage





Key features

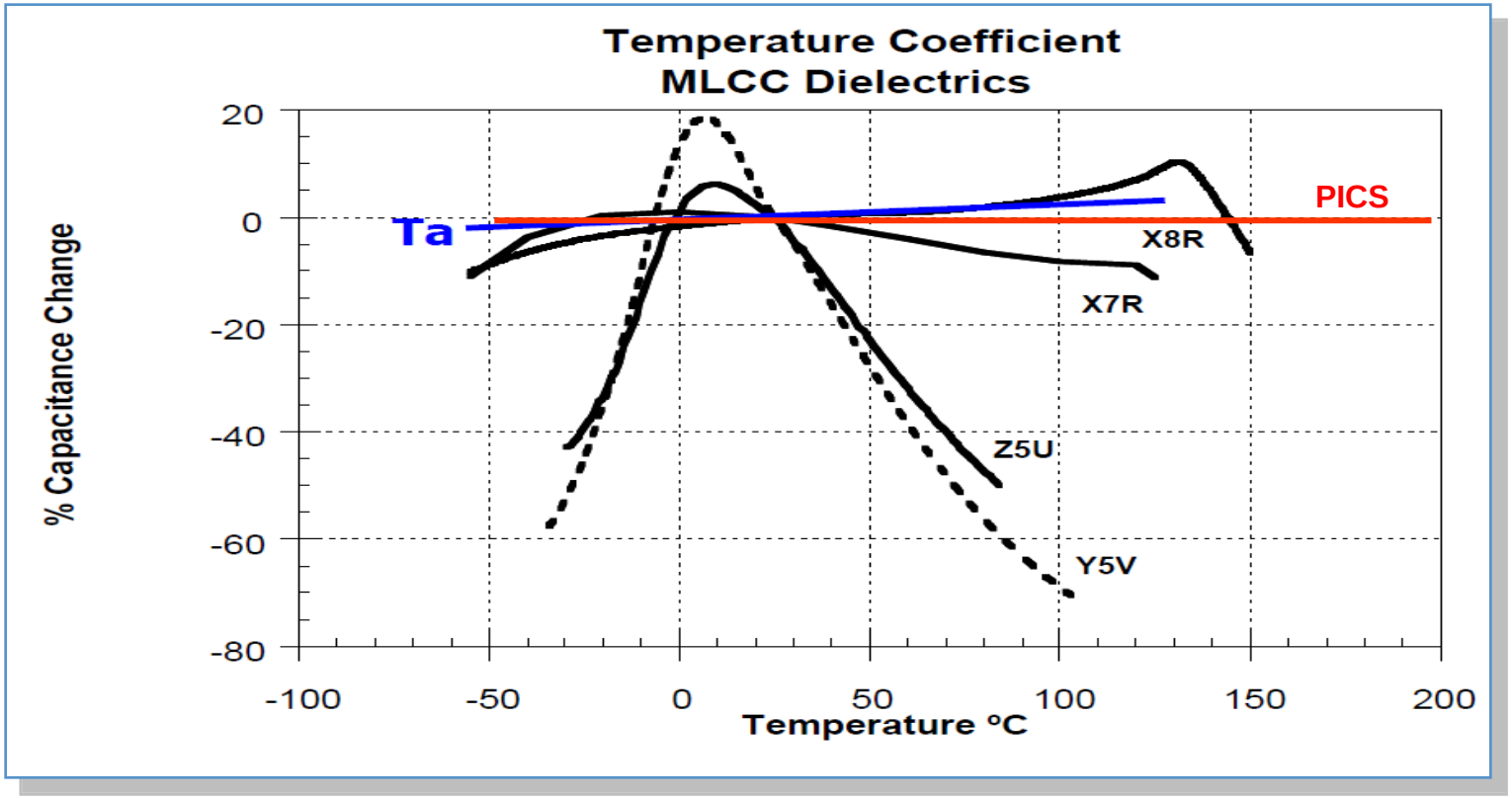
- 6 nf/ mm2 Operating voltage =30V , VBD= 100V
- Ground connection to the back of the Silicon capacitor
- Wirebond connection on top for the voltage line.
- Thickness 250 µm
- Lifetime extremely high

Performances

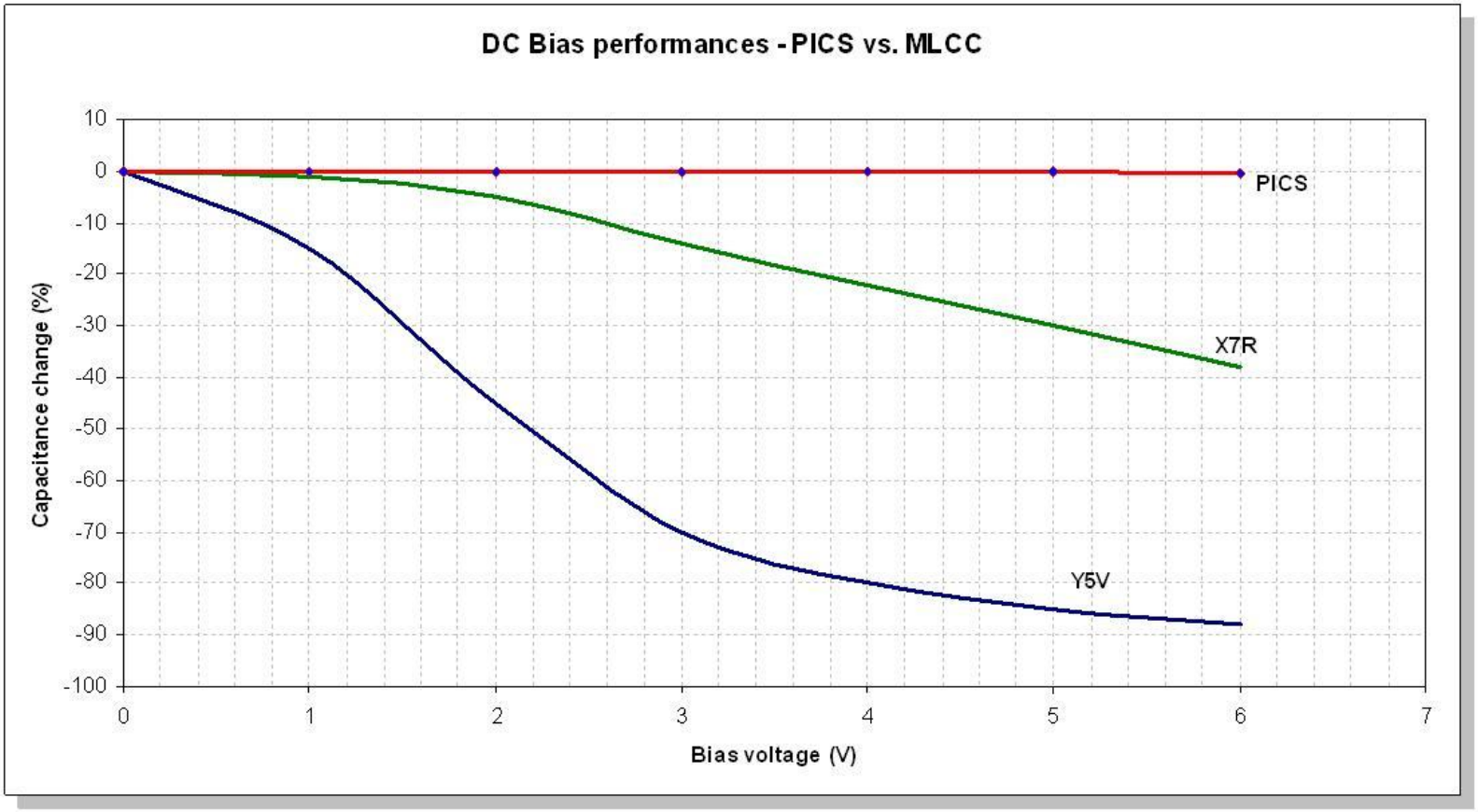
The IPDiA Silicon Capacitor technology offers several technical improvements over the MLCC technology :

- Stability over time and temperature, no aging, no capacitance shift
- Stability with applied voltage,no Voltage derating
- Very good matching capability, < 1.5% per array & tight distribution
- Much higher initial IR values (>1Gohm), no DC leakage
- Low parasitics
- Low thickness capability

High temperature capability of 200°C with no Capacitance shift



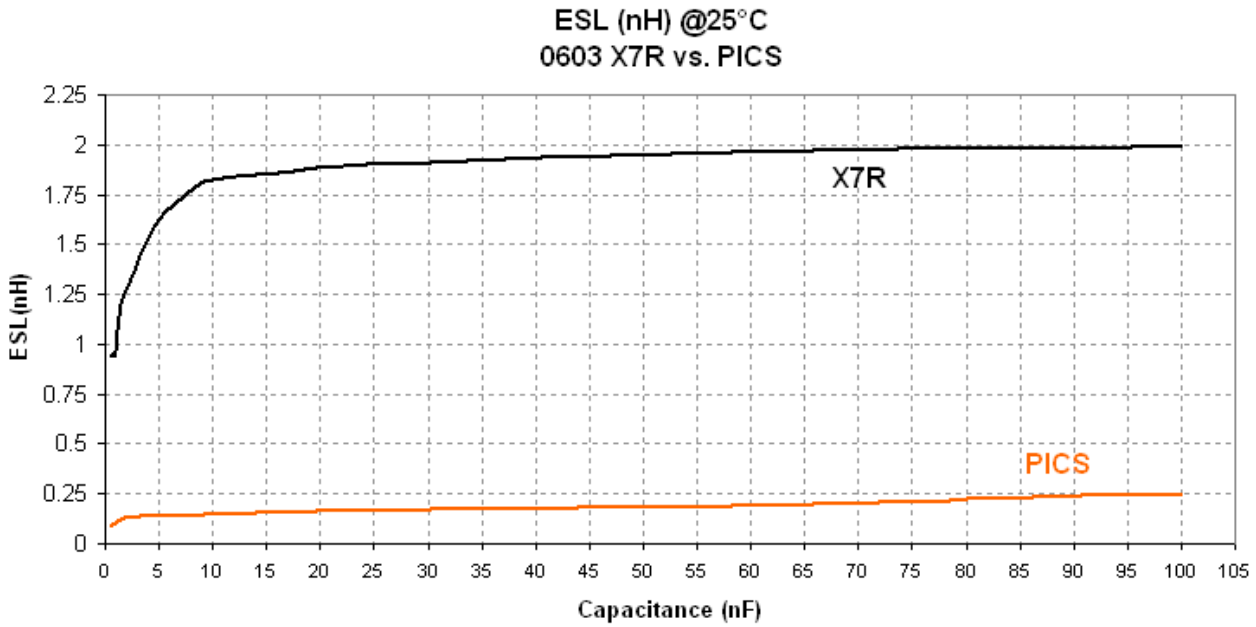
High temperature capability of 200°C with less than 0,1 % voltage derating



Example of a Capacitor of 100nF

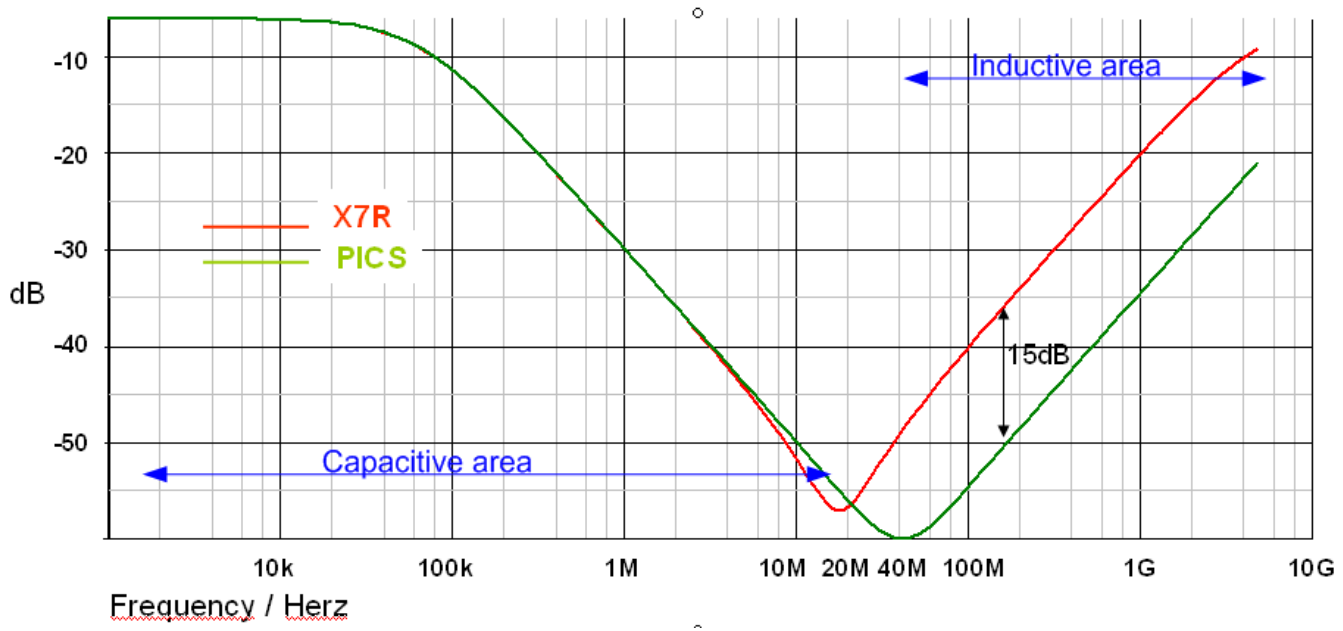
Low parasitics (ESR, ESL)

ESR<40mOhms
ESL<250pH
Q factor (>400)
Very good Capacitance stability vs frequency

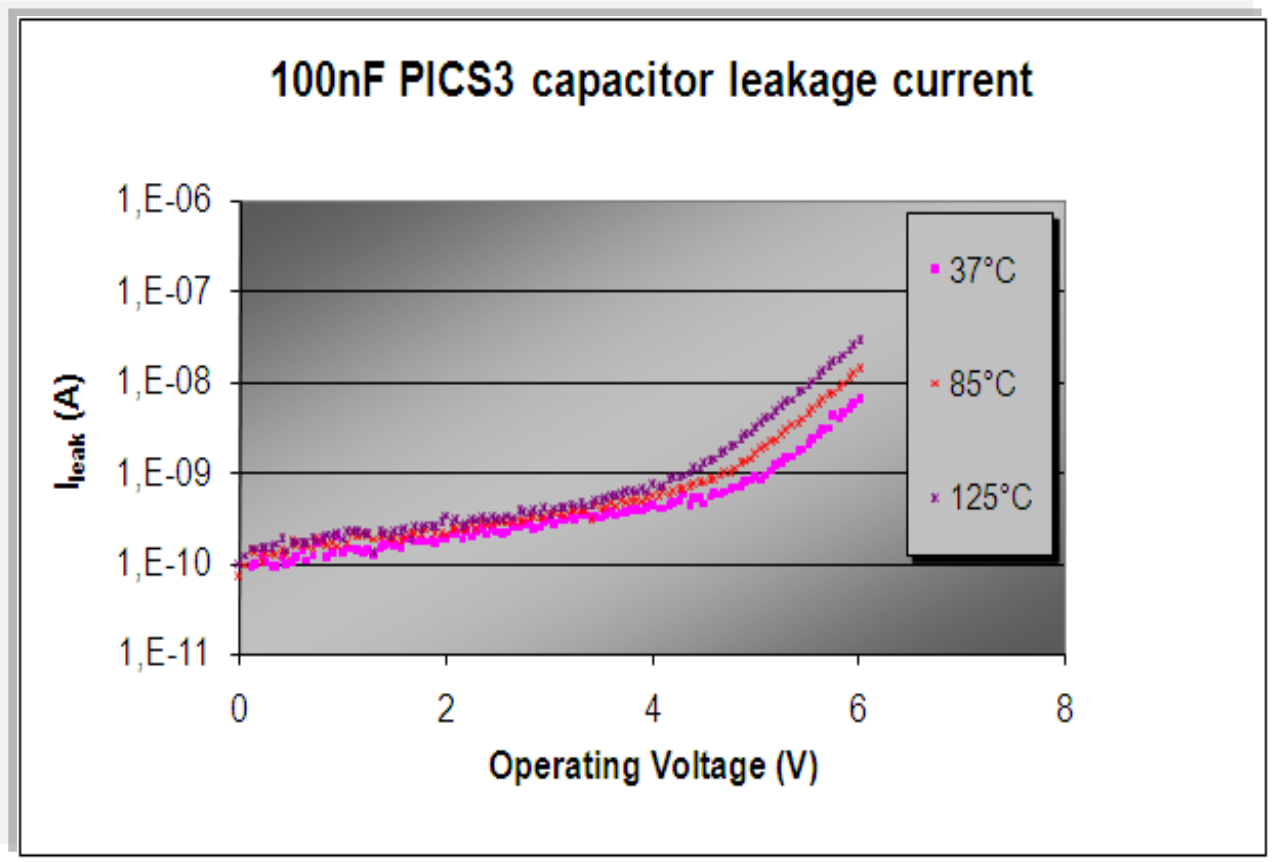


Application example: Power Supplies decoupling

Thanks to ultra low ESL performances, frequency rejections can be improved by 15dB.



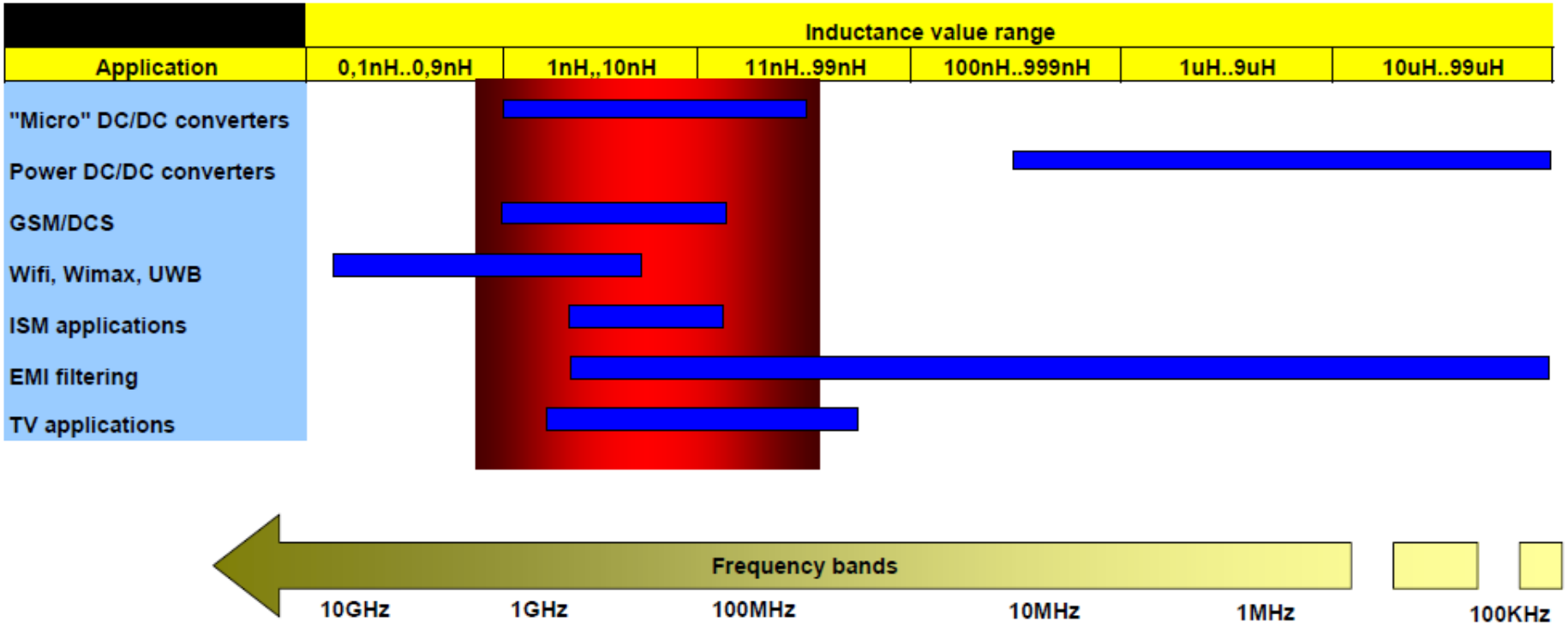
Low leakage current



Insulation resistance Between 2 caps is high > 50G ohm.µF

Leakage current is < 30nA/µF under normal operating voltage IR> 1Gohm

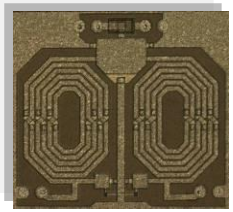
Inductor value vs Application/ Frequency band



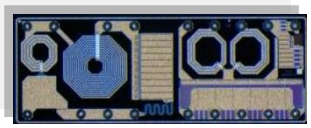
Other standard where our technology is: Bluetooth, Zigbee

Standard RF Silicon devices

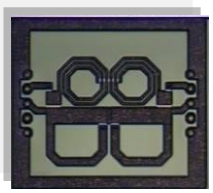
ISM Coupler



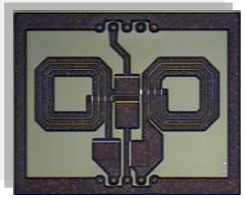
Companion for ISM tranceiver



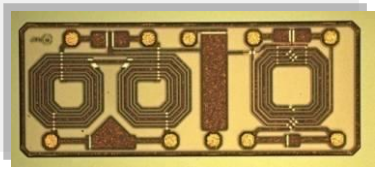
WLAN Band Pass Filter 2.4-2.5 GHz.



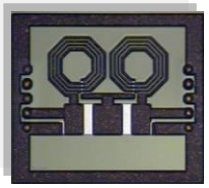
GSM/DCS Duplexer



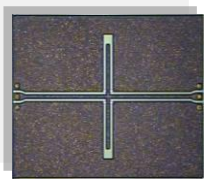
GSM Balun



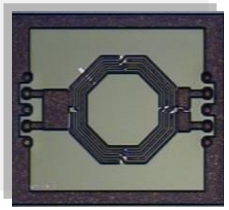
GSM Low Pass Filter



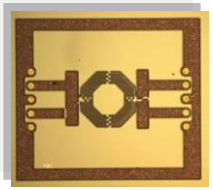
Stub for impedance matching at 70 GHz



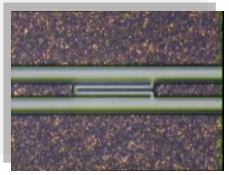
GSM LB Balun



UWB Balun



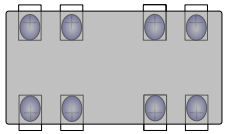
High frequency capacitor 80 GHz

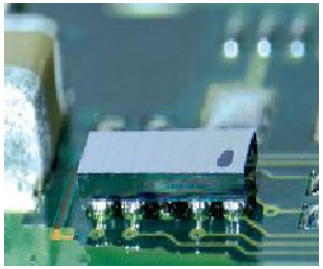


Packaging

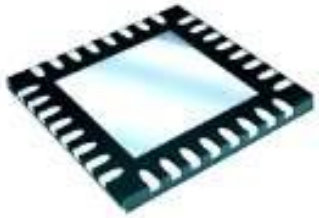
WL-CSP directly flipped on PCB :

Compatible with soldering technologies, such as wave soldering and reflow

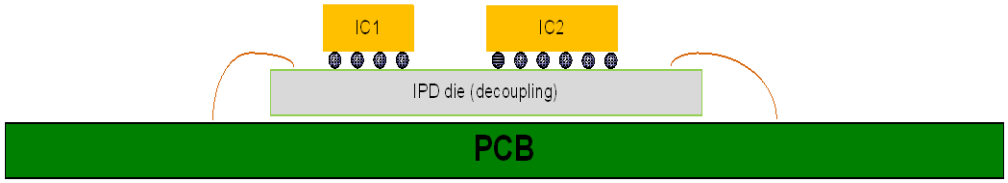


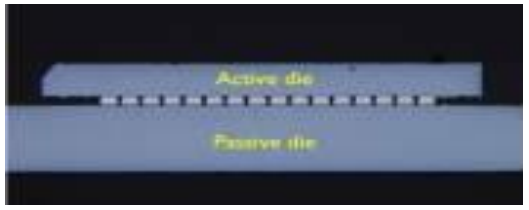


Companion chip (package)



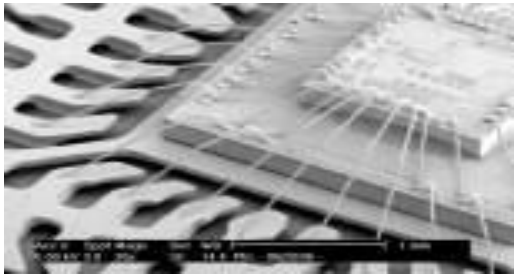
Active dies flip-chipped on IPD)



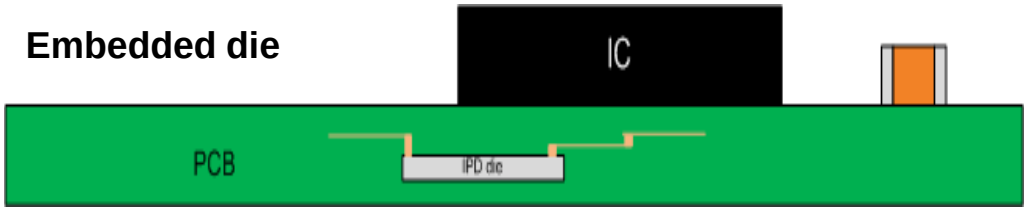


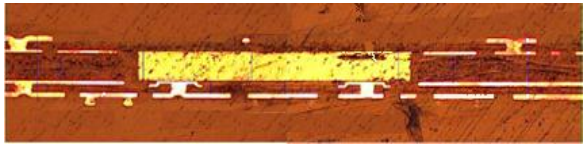
Packaging

Stacked dies)

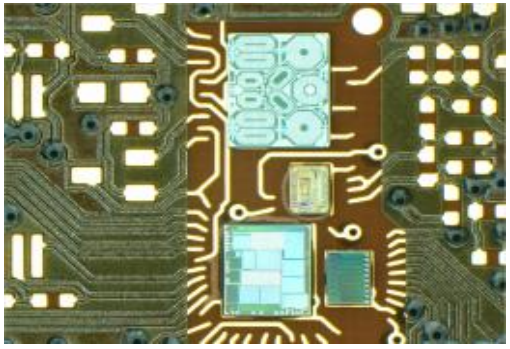


Embedded die



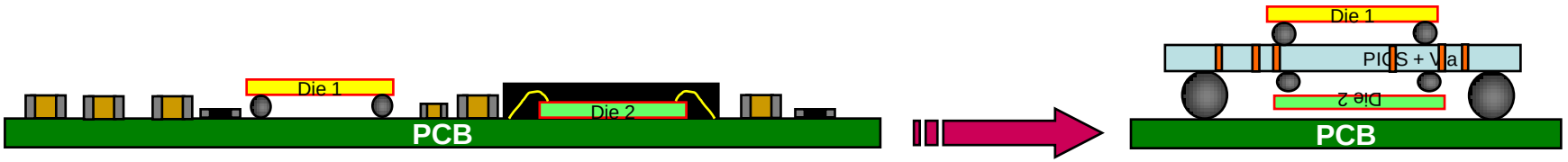


Chip on board (COB with globtop)

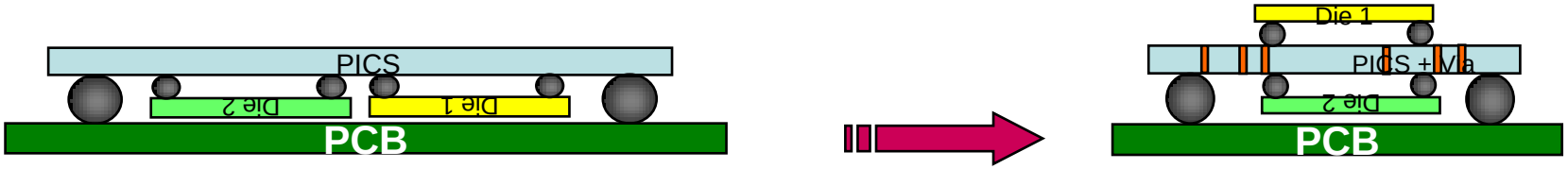


IPD with Through Silicon Vias

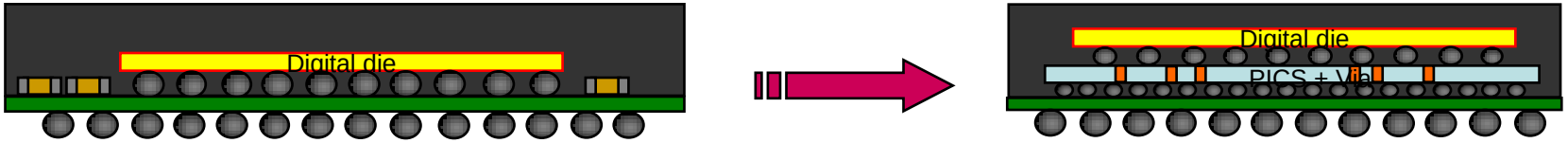
Situation I : Silicon Interposer for on board applications with SMDs



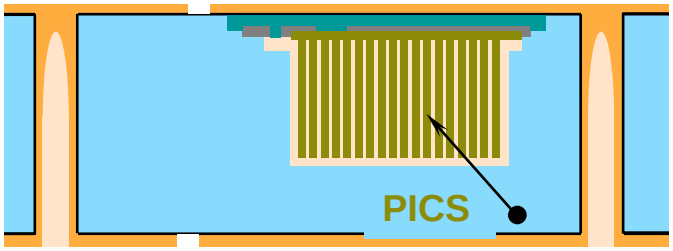
Situation II : Silicon Interposer for WLCSP SIP

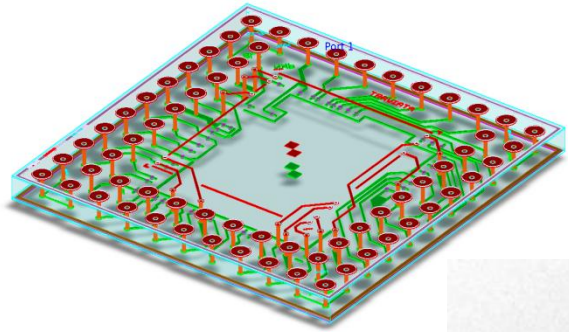


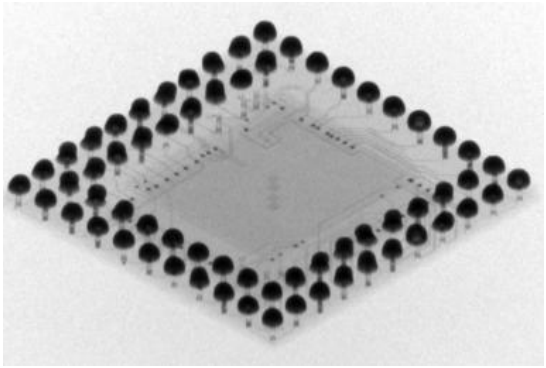
Situation III : Silicon Interposer for digital die

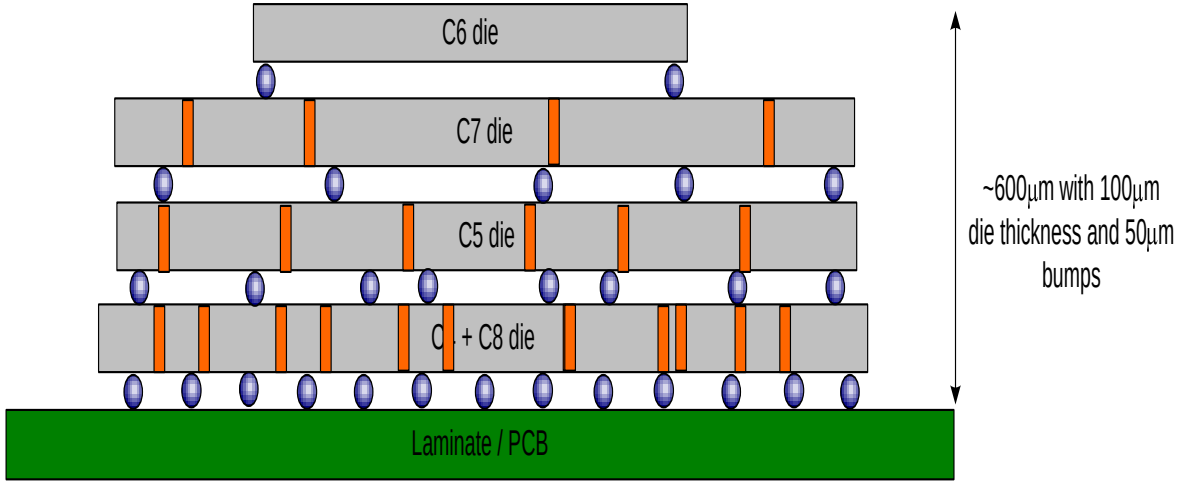


PICS with TSV

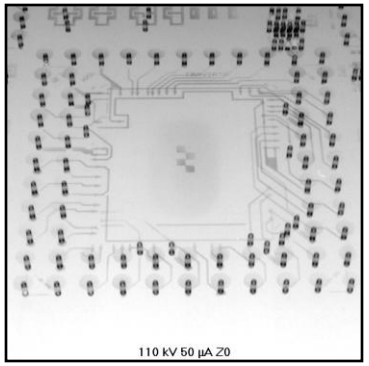


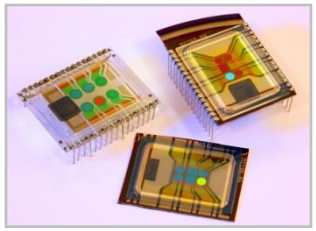






~600µm with 100µm die thickness and 50µm bumps





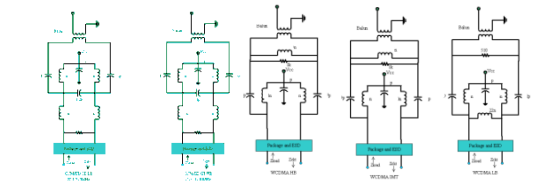
Custom products

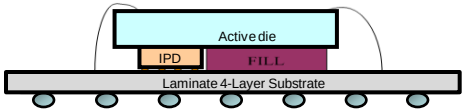
and

their application

ipdia
The 3D Silicon Leader

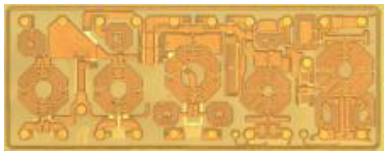
Custom PICS realization





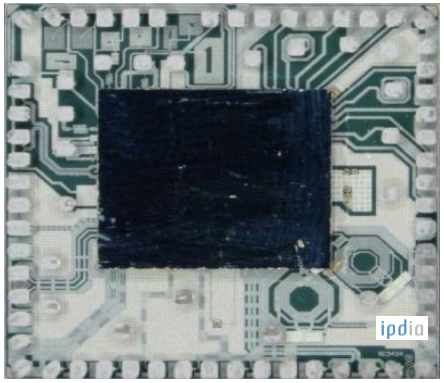
IPD RF module

Cellular (800MHz to 2GHz: W-CDMA)



1.5 mm x 5 mm

- **Balun array** flip chipped on laminate (SIP)
- Integration of 42 SMD (RF capacitors, Rf inductors, RF baluns & decoupling capacitors) for multi-band WCDMA transmitter



Active die flip-chipped on the IPD

5 mm x 5 mm

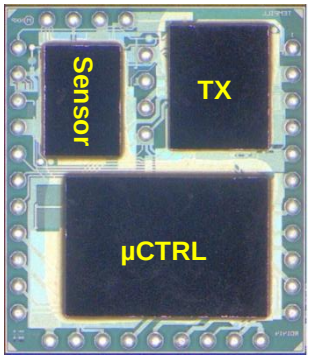
IPD RF module **(with 73 SMD embedded)**

- **Cellular** (passive part of W-CDMA & GSM RF transceiver)

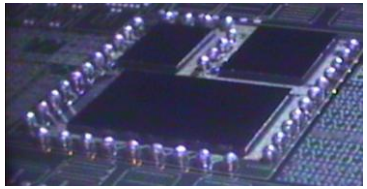
850-950MHz & 1.7-1.9GHz

- **RF Silicon carrier** flip chipped on lead frame (SIP)
- Components: RF capacitors, RF inductors, RF baluns, loop filters, decoupling capacitors and RF ESD protections.

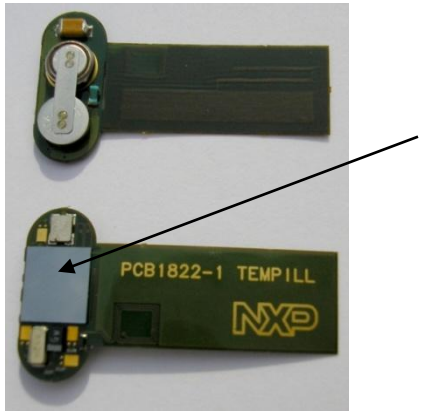
An electronic pill with a PICS die on Flex



3 Active dies flip-chipped on the IPD (7.00 x 7.00 mm)

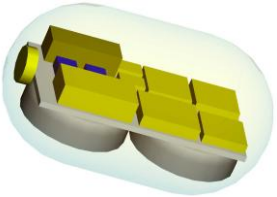


2nd interconnect bumps on IPD



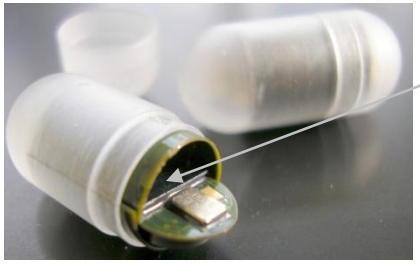
IPD

Double flip-chip on foil



- Market: **Medical**
- Application: **Temperature and medicine in-situ monitoring**
- 96 SMD components are integrated and composed of RF capacitors, decoupling capacitors, resistors, inductors, ESD diodes and PIN diodes.
- **3 actives die flipped** over an IPD Substrate including components and interconnects

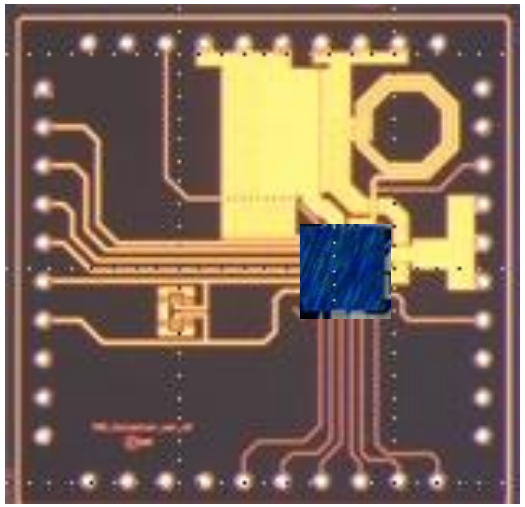
Module into electronic pill



IPD

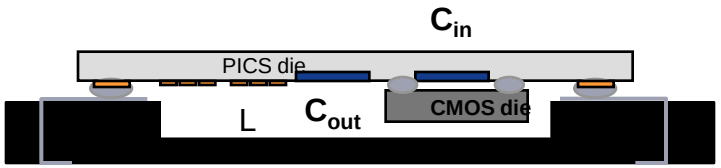
Electronic pill showing the IPD
(8 mm diameter x 17 mm long)

A DC/DC converter with PICS

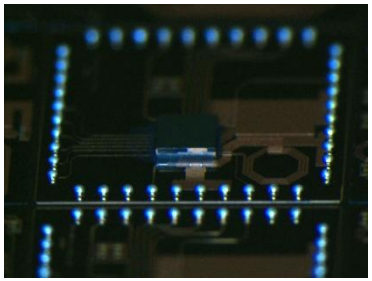


Active die flip-chipped on the IPD

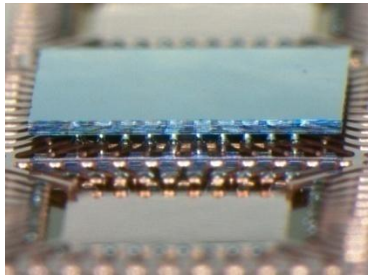
- Market Application: **Consumer**
- Frequency range: **100 MHz**
- Components: Resistors, capacitors, Inductor, Interconnects



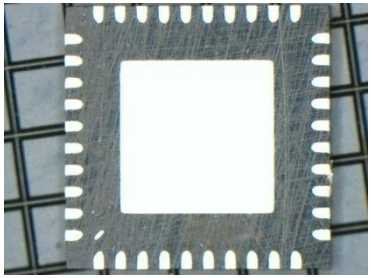
Module architecture



2nd interconnect bumps on IPD

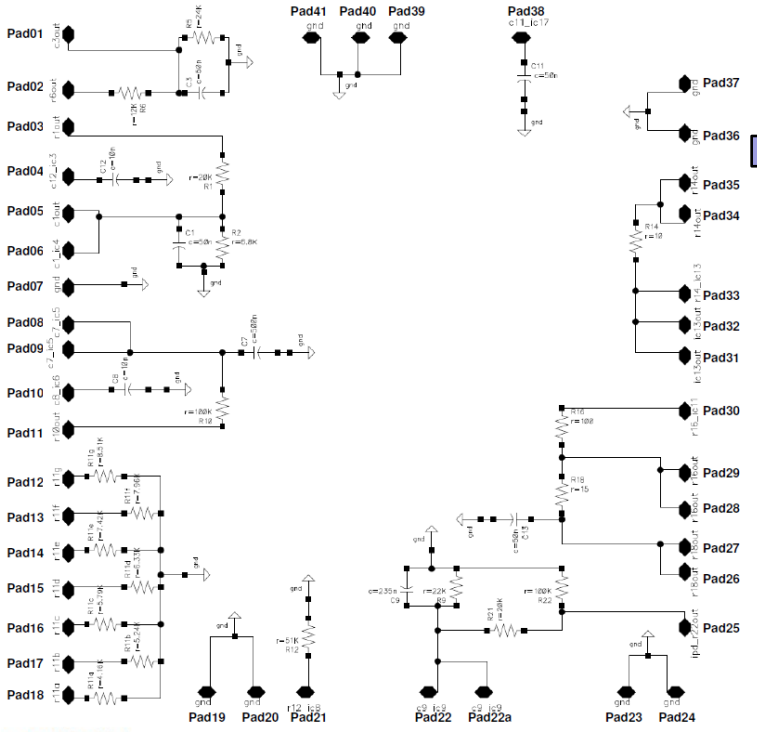


Double flip-chip on lead frame



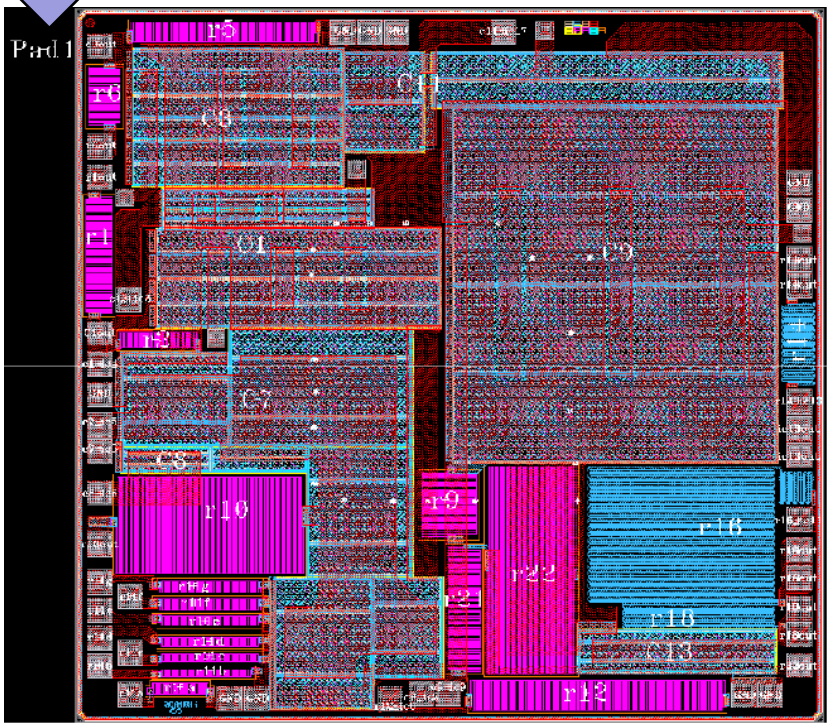
HVQFN40 final package

A DC/DC converter with PICS for a LED driver



- Die size:4.4 x 4.2mm
- 27 passive components

(19 resistors, 8 capacitors)



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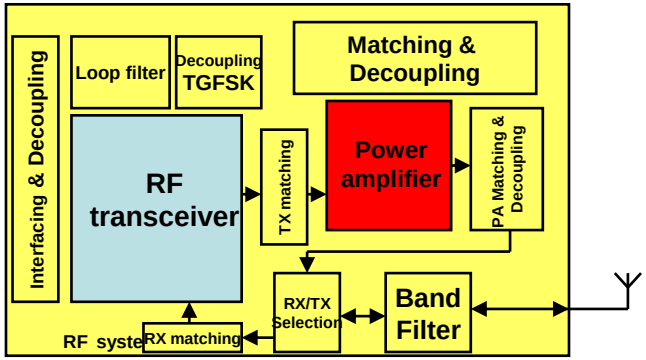
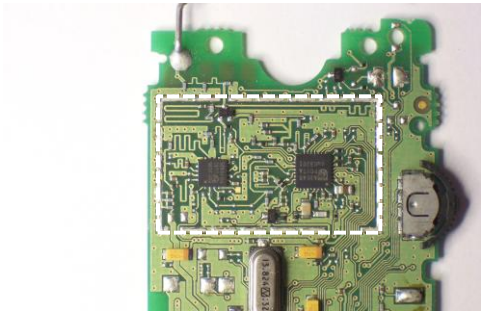
Full DECT RF Module



Full RF application block diagram

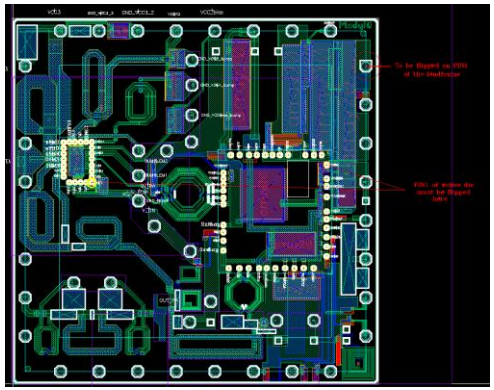
- Market Application: **Cordless**
- Frequency range: **1.8-1.9GHz (DECT)**
- Components: RF capacitors & matching, Decoupling capacitors, Inductors for balun, loop filter, serial resistors...



Previous RF application size

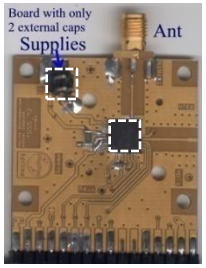
~450mm²

System in Package in a HVQFN32 package (5mm x 5mm)



IPD's layout

Assembly:
2 active dies flip-chipped on the IPD



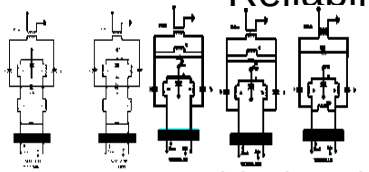
New RF application size

~30mm²

Only one HVQFN chip
+
2 external capacitors

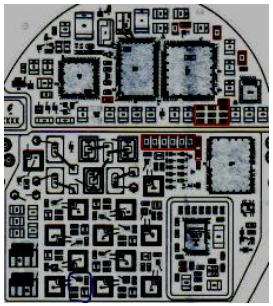
Checklist to start a study

- More information we will have, deeper the analysis will be…
  - Application domain
  - Electrical schematics
  - Application layout
  - Pictures, datasheet
  - Bill Of Materials (capacitor size, type, quantity, price, from which company…)
  - Voltage supply and electrical signals (Voltage, current, frequency, duty-cycle…)
  - Life time
  - Reliability

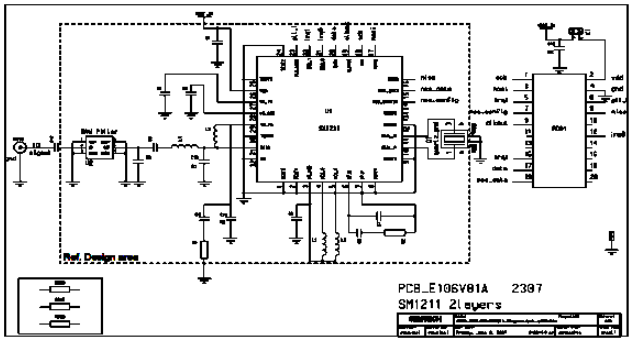


Partial Schematic

Micro photograph of application



Complete layout of application



Complete schematic of application

Value	Tol +/- (%)	Description	Die structure	Die size
3 x 3.3 pF	15	Capacitor array	C	A = 500µm
3 x 8.2 pF	15	Capacitor array	C	A = 500µm
3 x 12 pF	15	Capacitor array	C	A = 500µm
3 x 100 pF	15	Capacitor array	C	A = 500µm
2 x 330 pF	15	Capacitor array	B	A = 500µm
2 x 470 pF	15	Capacitor array	B	A = 500µm
1 nF	15	Single capacitor	A	A = 500µm
4 x 4.7 nF	15	Capacitor array	D	A = 1000µm
4 x 10 nF	15	Capacitor array	D	A = 1000µm
2 x 33 nF	15	Capacitor array	B	A = 1000µm
100 nF	15	Single capacitor	A	A = 1000µm
0.25pF, 0.5pF, 1pF, 2pF, 4pF	15*	Binary capacitor n° 1	E	A = 1000µm
8pF, 16pF, 32pF, 64pF, 128pF	15	Binary capacitor n° 2	E	A = 1000µm

*15% not guarantee for 0.25pF capacitor value

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Conclusion

- The technology is proven is the consumer market
- It's being adopted in the medical domain
- We are adapting our technology to the customer needs to make it a success

Thanks for your attention

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